AMENDMENTS

Please amend the following claims, wherein strikethrough denotes deletions and underlining denotes additions.

1. (Currently Amended) An exponent computation apparatus for performing overflow and underflow comparisons while minimizing overflow/underflow comparison circuitry, said apparatus comprising:

overflow/underflow possible check circuitry, said overflow/underflow possible check circuitry configured to determine if a mathematical operation involving a first exponent signal and a second exponent signal creates a potential overflow condition, wherein said overflow/underflow possible check circuitry is configured to generate a underflow/overflow signal indicating if said overflow condition is a possibility and generate an exponent selection signal, and wherein said exponent selection signal is indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and is indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal; and

exponent compare circuitry configured to compute an actual overflow/underflow condition for said first or second exponent signal based upon said exponent selection signal, said exponent compare circuitry configured to compute an actual overflow condition if said underflow/overflow signal indicates overflow is possible, said exponent compare circuitry configured to compute an actual underflow condition if said underflow/overflow signal does not indicate overflow is possible.

2. (Original) The apparatus of claim 1, wherein said exponent compare circuitry generates an error signal if an actual overflow/underflow condition exist.

3. (Original) The apparatus of claim 2, further comprising:

a pre-normalized exponent selection circuitry configured to determine a larger exponent between said first exponent signal and said second exponent signal.

4. (Original) The apparatus of claim 3, wherein said overflow/underflow possible check circuitry uses said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

5. (Original) The apparatus of claim 3, further comprising:

an exponent shift amount circuitry configured to determine how much the mantissa of said largest exponent must be shifted to be normalized, and configured to compute a normalized exponent.

6. (Original) The apparatus of claim 5, wherein said exponent compare circuitry uses said normalized exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

7. (Currently Amended) A method for performing overflow and underflow comparisons with exponent comparison circuitry, comprising the steps of:

determining if a mathematical operation creates a potential overflow condition;

generating an underflow/overflow signal indicating if said potential overflow condition exists;

determining which of said first and second exponent signals is greater;

generating, based on said determining step, an exponent selection signal indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal;

computing an actual overflow condition for said first or second exponent signal based upon said exponent selection signal with said exponent comparison circuitry if said underflow/overflow signal indicates that a potential overflow condition exists; and

computing an actual underflow condition for said first or second exponent signal based upon said exponent selection signal with said exponent comparison circuitry if said underflow/overflow signal indicates said potential overflow condition does not exist.

8. (Previously Presented) The method of claim 7, further comprising the steps of:

generating an overflow error signal if an actual overflow condition exists; and

generating an underflow error signal if an actual underflow condition exists.

9. (Original) The method of claim 7, further comprising the step of:

determining a largest exponent between said first exponent signal and said second exponent signal.

10. (Original) The method of claim 9, further comprising the step of:

using said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

11. (Original) The method of claim 9, further comprising the steps of:

determining how much a mantissa of said largest exponent must be shifted to be normalized, and

computing a normalized exponent.

12. (Original) The method of claim 11, further comprising the steps of:

using said normalized exponent to determines if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

13. (Currently Amended) An exponent computation apparatus for performing overflow and underflow comparisons while minimizing overflow/underflow comparison circuitry, the apparatus comprising:

means for determining if a mathematical operation creates a potential overflow condition;

means for generating an underflow/overflow signal indicating if said potential overflow condition exists;

means for generating an exponent selection signal, said exponent selection signal indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal; and

means for computing an actual overflow condition for said first or second exponent signal based upon said exponent selection signal if said underflow/overflow signal indicates said potential overflow condition exists and an actual underflow condition for said first or second exponent signal based upon said exponent selection signal if said signal indicates said potential overflow condition does not exist.

14. (Original) The apparatus of claim 13, wherein said computing means further comprises:

means for generating an overflow error signal if an actual overflow condition exist; and

means for generating an underflow error signal if an actual underflow condition exist..

15. (Original) The apparatus of claim 13, further comprising:

means for determining a largest exponent between said first exponent signal and said second exponent signal.

16. (Original) The apparatus of claim 13, wherein said computing means further comprises:

means for using said largest exponent to determine if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

17. (Original) The apparatus of claim 14, further comprising:

means for determining how much a mantissa of said largest exponent must be shifted to be normalized, and

computing a normalized exponent.

18. (Original) The apparatus of claim 17, wherein said computing means further comprises:

means for using said normalized exponent to determines if said mathematical operation between said first exponent signal and said second exponent signal creates said overflow condition.

Claims 19-29. (Cancelled)

30. (Currently Amended) ~~An apparatus~~The apparatus of claim 1, wherein the exponent compare circuitry is further configured to perform multiple simultaneous compares of an exponent and a plurality of overflow thresholds, if said signal indicates the possibility of an overflow.

31. (Currently Amended) ~~An apparatus~~The apparatus of claim 1, wherein the exponent compare circuitry is further configured to perform multiple simultaneous compares of an exponent and a plurality of underflow thresholds, if said signal indicates the possibility of an underflow.

32. (Previously Presented) A method for performing overflow and underflow comparisons with exponent comparison circuitry, comprising the steps of:

selecting an exponent precision underflow/overflow constant from a plurality of exponent underflow/overflow constants;

generating a sum signal and a carry signal from one of said plurality of exponent underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal;

computing an underflow/overflow result from said sum signal and said carry signal; and

transmitting an underflow/overflow condition based upon said underflow/overflow result and an exponent adjust amount signal.

33. (Currently Amended) The method of ~~claim 33~~claim 32, wherein the selecting step further comprises selecting said constants via a plurality of constant selectors.

34. (Currently Amended) The method of ~~claim 34~~claim 33, wherein said plurality of constant selectors comprises two constant selectors.

35. (Currently Amended) The method of ~~claim 35~~claim 34, wherein the generating step further comprises generating said sum signal and said carry signal via a plurality of carry save adders.

36. (Currently Amended) The method of ~~claim 36~~claim 35, wherein the computing step further comprises computing said underflow/overflow result via a plurality of comparators.

37. (Currently Amended) The method of ~~claim 37~~claim 36, wherein said plurality of comparators further comprises four comparators and wherein a first one of said four comparators uses a least significant bit input of said carry signal from one of said plurality of carry save adders and a carry-in signal to extend the range of said constants being compared.

38. (Previously Presented) The apparatus of claim 1, wherein said exponent compare circuitry comprises a plurality of underflow/overflow result selectors, each result selector configured to transmit said overflow condition and said underflow condition based upon an underflow/overflow result from a plurality of comparators and further based upon an exponent adjust amount signal.

39. (New) The apparatus of claim 1, wherein said computation of said portion of said mathematical operation is performed via a carry save adder and a comparator.